AMENDMENTS TO THE SPECIFICATION

In the Specification:

Please replace the paragraph beginning on page **11**, line **23** with the following rewritten paragraph:

-- Once the critical interconnects, including those affected by crossing lines, have been identified, a T-line model is defined for each of the critical interconnects as indicated by step 23 in Figure 3. For each critical interconnect, a T-line structure is first defined. In this embodiment, the T-line structure for an interconnect is defined by selecting a desired structure from a predefined set of parameterized structures in modeling component 13 of component library 11. An example of a set of structures which might be employed here is shown in Figures 4a through 4f. The structures 30a through 30f illustrated in these figures correspond to those described in the references given above for our earlier interconnect-aware design system. Each figure shows a cross-section of the basic geometry of the structure (see the upper component marked in sideways lines in Fig. 4a), defining the arrangement of signal wires, shielding and (in Figures 4b and 4d) vias, with general parameters corresponding to dimensions such as width, thickness, height and separation of the various elements. These dimensions are represented by parameters w, th, h, th_g, Wg, Ws, s and d in the set of structures as illustrated in the figures. A basic characteristic of these structures is that they conform to the closed environment condition discussed earlier, whereby most of the electric field lines and the current return path are contained within the structure boundary. In the examples shown, structures 30a through 30d are microstrip structures, and structures 30e and 30f are coplanar (CPW) structures. Of the microstrip structures, structures 30a and 30b are single-wire T-line structures, and structures 30c and 30d are two-coupled-wire structures particularly suitable for differential designs. The microstrip structures 30a through 30d here include a bottom shielding layer to inhibit coupling to the conductive silicon substrate (not shown), and thus inhibit substrate cross-talk, while also reducing inductance of the structure and thus reducing inductance-related signal integrity problems such as overshoots, ringing and damped resonances in longer wires. Structures 30b and 30d also include side shielding of the signal line, with optional stacked vias being included here between the side and bottom shielding ensuring equal potential on the bottom and side shields, since the via to via

separation is designed to be smaller than the shortest possible on-chip wavelength. The coplanar structures 30e (single-wire) and 30f (two-coupled-wire) have only side shielding. This offers extra design flexibility and may be particularly useful for CMOS high-density designs where the use of bottom shielding may present design difficulties.--